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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/758,841

01/16/2004

Ching Hsiang Yang

407200

6961

7590

09/28/2004

Harold V. Stotland
Seyfarth Shaw
42nd Floor
55 East Monroe Street
Chicago, IL 60603-5803

EXAMINER

JEANGLAUDE, JEAN BRUNER

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/758,841

Applicant(s)

YANG ET AL.

Examiner

Jean B Jeanglaude

Art Unit

2819



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-9 is/are allowed.
- 6) ☒ Claim(s) 10 is/are rejected.
- 7) ☒ Claim(s) 11-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>1-16-04</u> . | 6) <input type="checkbox"/> Other: _____ |

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's admitted prior art in view of Ausserlechner et al. (US Patent Number 6,621,334).

3. Regarding claim 10, the APA discloses a constant current source with threshold voltage and channel length modulation (fig. 3, paragraph bridging pages 2 and 3) comprising a set of cascade transistors (fig. 3) including a first MOS transistor (M1) and a second MOS transistor (M2). The Applicant's admitted prior art does not implicitly disclose a constant current source with threshold voltage and channel modulation that comprises a compensation circuit electrically connected to the first MOS and second MOS transistors so as to form a feedback circuit. However, Ausserlechner et al., in a related field, discloses a system (fig. 7) in which compensation circuit (C1 and C2 form the compensation circuit) that is connected to the transistors (T1, T2) that forms a feedback circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Ausserlechner et al.'s system in the Applicant's admitted prior art in order to operate a frequency compensated amplifier configuration in which constructing the amplifier involves taking into account the actual useful signal bandwidth (col 3, lines 23 – 52).

Allowable Subject Matter

Claims 1 – 17 are allowable.

The following is a statement of reasons for the indication of allowable subject matter: in combination with other limitations of the claims the prior arts made of record fail to suggest a constant current source with threshold voltage and channel length modulation that comprises a third MOS transistor including a gate terminal, a first terminal and a second terminal, wherein the gate terminal and the first terminal are coupled to the gate terminal of a second MOS transistor; a fourth MOS transistor including a gate terminal, a first terminal and a second terminal, wherein the gate terminal and the first terminal are coupled to the gate terminal of a first MOS transistor and the second terminal of the third MOS transistor and the second terminal is coupled to a first reference voltage.

4. Claims 11 – 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Miki et al. (US Patent Number 5,517,152) discloses a current source circuit and operating method thereof.

7. McClure (US patent Number 5,598,122) discloses a voltage reference circuit having a threshold voltage shift.

8. Gross (US Patent Number 5,619,166) discloses an active filtering method and apparatus.
9. Werking (US Patent Number 5,798,658) discloses a source-coupled logic with reference-controlled inputs.
10. Masuda (US patent Number 6,008,679) discloses a semiconductor integrated circuit and semiconductor input system.
11. Ishii (US patent Number 6,081,131) discloses a logical amplitude level conversion circuit, liquid crystal device and electronic apparatus.
12. Kirsch et al. (US patent Number 6,320,417) discloses a multi-bit, current mode data bus.
13. Taylor (US patent Number 5,936,392) discloses a current source, reference voltage generator, method of defining a PTAT current source and method of providing a temperature compensated reference voltage.
14. Kiyose (US Patent Number 6,515,520) discloses a charge pump circuit for phase-locked loop circuitry.
15. Oikawa (US Patent number 6,587,000) discloses a current source mirror circuit and ADC.
16. Kimura (US Patent Number 6,657,485) discloses a linear voltage subtractor/Adder circuit and MOS differential amplifier circuit therefor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-

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272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jean Bruner Jeanglaude
Primary Examiner
September 14, 2004